WHAT IS CLAIMED IS:

1. A thin film transistor array panel comprising:

an insulating substrate;

a pair of first and second signal lines formed on the insulating substrate;

a third signal line formed on the insulating substrate and intersecting the first and the second signal lines in an insulating manner;

a fourth signal line formed on the insulating substrate and intersecting the ~~second~~ third signal line in an insulating manner;

a pixel electrode formed in a pixel area defined by the intersections of the first and the second signal lines and the third signal line and including a plurality of subareas partitioned by cutouts;

a direction control electrode formed in the pixel area and including a portion overlapping at least one of the cutouts;

a first thin film transistor connected to the pixel electrode, the first signal line, and the third signal line;

a second thin film transistor connected to the pixel electrode, the second signal line, and the third signal line; and

a third thin film transistor connected to the direction control electrode, the second signal line, and the fourth signal line.

2. The thin film transistor array panel of claim 1, wherein the fourth signal line includes a portion overlapping at least one of the cutouts which does not overlap the direction control electrode.

3. The thin film transistor array panel of claim 2, further comprising a fifth signal line placed between the first and the second signal lines, wherein the fourth signal line is located between the first and the second signal lines and the fourth and the fifth signal lines have inversion symmetry.